**What is Claimed is:**

1.A method of generating a slicing table of fault distribution comprising:

a. dividing a memory into a number of memory pages of a predetermined size;

b. calculating a fault quantity for each $4k*2^n$ range according to statistic data of a memory fault distribution;

c. making a number of divisions using a range of the memory pages as a partition unit; and

d. posting a number of fault memory pages and arranging a number of associate memories and comparators to preserve a address bits of the fault memory pages and comparators.

2. The method of Claim 1, wherein in step b, n is an integer which is more than or equals to 0, so that ranges include 4K, 8K, 16K, 32K, 64K, and 128K.

3. The method of Claim 1, wherein in step c, when n is 1, the partition unit constitutes 8k memory pages, two of the fault memory pages are set to be tolerant, and two of the associate memories and comparators are arranged in step d.

4. The method of Claim 1, wherein in the step c, when n is 2, the partition unit constitutes 16k memory pages, two of the fault memory pages are set to be tolerant, and two of the associate memories and comparators are arranged in step d.

5. The method of Claim 1, wherein in the step c, when n is 3, the partition unit constitutes 32k memory pages, two of the fault memory pages are set to be tolerant, and two of the associate memories and comparators are arranged in step d.

6. The method of Claim 1, wherein in step c, when n is 5, the partition unit constitutes 128k memory pages, four of the fault memory pages are set to be tolerant, and four of the associate memories and comparators are arranged in step d.

7. The method of Claim 1, wherein the slicing table of fault distribution is built in a memory chip.

8. A structure of repairing a SDRAM by generating a slicing table of fault distribution comprising:

a plurality of address limiters being provided to restrict a address bits of a block when faults exceed a partition limit according to the slicing table of fault distribution and to repair the faults by using a fault limit of another partition with a lower fault rate;

a plurality of associate memories being provided to preserve the address bits of a fault memory page, a number corresponds to a tolerant fault of a partition area;

a plurality of comparator arrays being provided to compare an input

address bits with an output address bits of an address limit to determine different ranges of memory address bits, decide whether any default exists, and generate a fault signal transferred to an encoder;

a encoder being provided to set up a repair address bits associate with a repair memory after receiving said fault signal; and

a repair memory being provided to point a memory page address bits generated by said encoder to a new remapping address bits as to preserve the data.

9. The structure of Claim 8, further comprising a multiplexer being provided to be controlled by the fault enable signal generated by said comparator arrays, so that the system read data from the original address bits or the remapping address bits.

10. The structure of Claim 8, wherein the repair address bits comprises a column of the address bits and a validation column.

11. A method of repairing a SDRAM by generating a slicing table of fault distribution comprising:

a. booting a system;

b. executing a memory test to find an address and distribution of a fault in the memory chip;

c. if the fault distribution is in the planned range in advance, establishing the slicing table of fault distribution;

d. if the fault distribution is concentrated in a predetermined range, establishing the slicing table of fault distribution and posting address limits;

e. inputting a address bits into the address limits;

f. using comparator arrays to check whether an input address bits is in different address bits ranges according to the slicing table of fault distribution;

g. if there are no faults, mapping the input address bits to the SDRAM and reading data at the mapping address bits;

h. if there are faults, a fault enable signal is generated, so that data at the original input address bits are not read and a fault signal is transferred to an encoder;

i. using said encoder to set up a repair address bits for the fault;

j. pointing a repair memory to a new remapping address bits according to the repair address bits;

k. replacing the original input address bits with the remapping address bits; and

l. reading data at the remapping address bits in the SDRAM.